

Electronic Devices & Circuits ①

1a) V_T is voltage equivalent of temperature
The dependence of I_0 and V_T on temperature
T is given by.

$$I_0 = k T^m e^{-V_{G0}/nV_T} \quad \text{--- (1)}$$

k = const dependent on temp.
 $m = 2$ for Ge and 1.5 for Si

V_{G0}/E_{G0} = Forbidden energy gap
= 0.785V for Ge.
= 1.21V for Si

→ from eq (1) as temp increases, the value
of I_0 increases hence diode current I
increases.

→ To keep diode current constant, it is
necessary to reduce the applied voltage
V of the diode. ($\frac{dI}{dT} = 0$)

$$I = I_0 \left[e^{(V/nV_T)} - 1 \right]$$

$$I \approx I_0 e^{V/nV_T} \quad \text{--- (2)}$$

Sub (1) in (2)

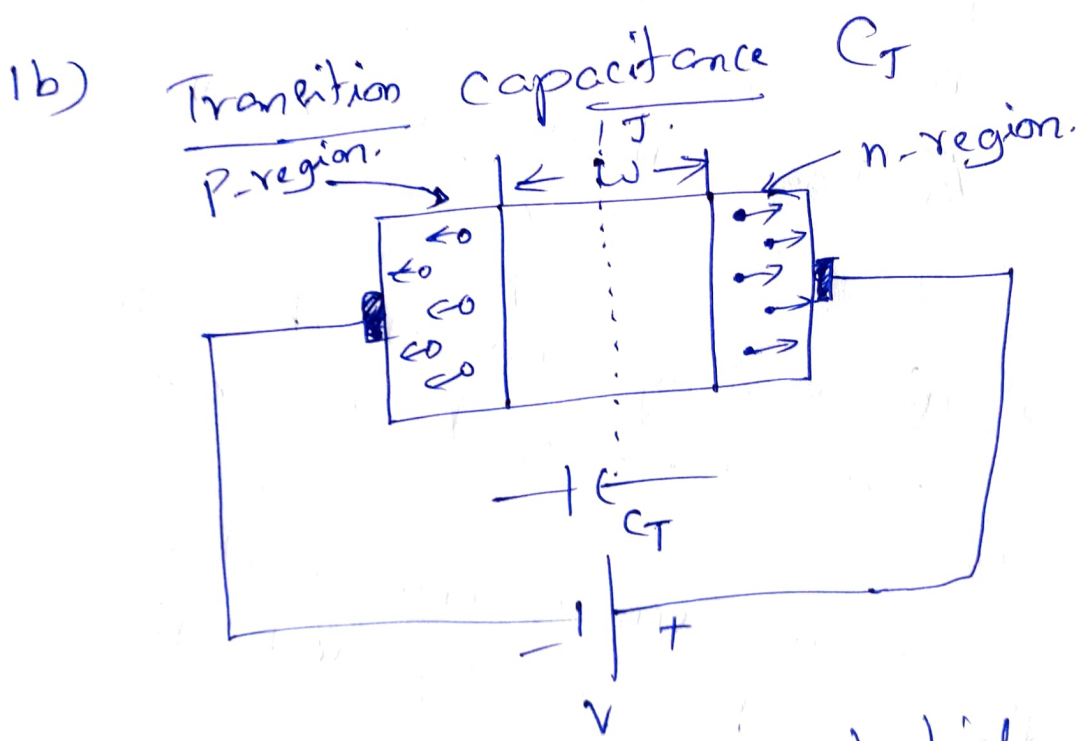
$$I = k T^m e^{-V_{G0}/nV_T} \cdot e^{V/nV_T}$$

$$\therefore I = kT^m e^{(V-V_{G0})/nV_T} \quad (V_T = kT) \quad \underline{\underline{3m}} \quad \textcircled{2}$$

diff the above equation with respect to T

$$\frac{dI}{dT} = k \left[m T^{m-1} e^{(V-V_{G0})/nV_T} + T^m e^{(V-V_{G0})/nV_T} \frac{d}{dT} \left(\frac{V-V_{G0}}{nV_T} \right) \right]$$

$$\therefore \frac{dV}{dT} = \frac{V - (V_{G0} + m n V_T)}{T} \quad \underline{\underline{2m}}$$



The relationship between potential and charge density is given by poisson's eq

$$\epsilon_0 \frac{d^2 V}{dx^2} = \frac{qNA}{E} \quad \textcircled{1}$$

Integrating the above equation

$$\int \frac{dV}{dx} = \frac{q N_A}{\epsilon}$$

$$\frac{dV}{dx} = \frac{q N_A x}{\epsilon}$$

Again Integrating.

$$\int \frac{dV}{dx} dx = \int_0^w \frac{q N_A}{\epsilon} x dx$$

$$\boxed{V = \frac{q N_A}{\epsilon} \frac{w^2}{2}} \quad \text{--- ②}$$

3M

The net charge Q

$$Q = N_A \cdot \text{Volume} \times q$$

$$Q = N_A A \cdot w \cdot q$$

differentiating q @ wrt V

$$1 = \frac{1}{2} \frac{N_A q}{\epsilon} \left[\frac{dw}{dV} \right] 2w$$

$$\frac{dw}{dV} = \frac{\epsilon}{q N_A w}$$

$$\frac{dQ}{dV} = N_A A q \frac{dw}{dV}$$

$$\frac{dQ}{dV} = N_A A q \cdot \frac{\epsilon}{q N_A w}$$

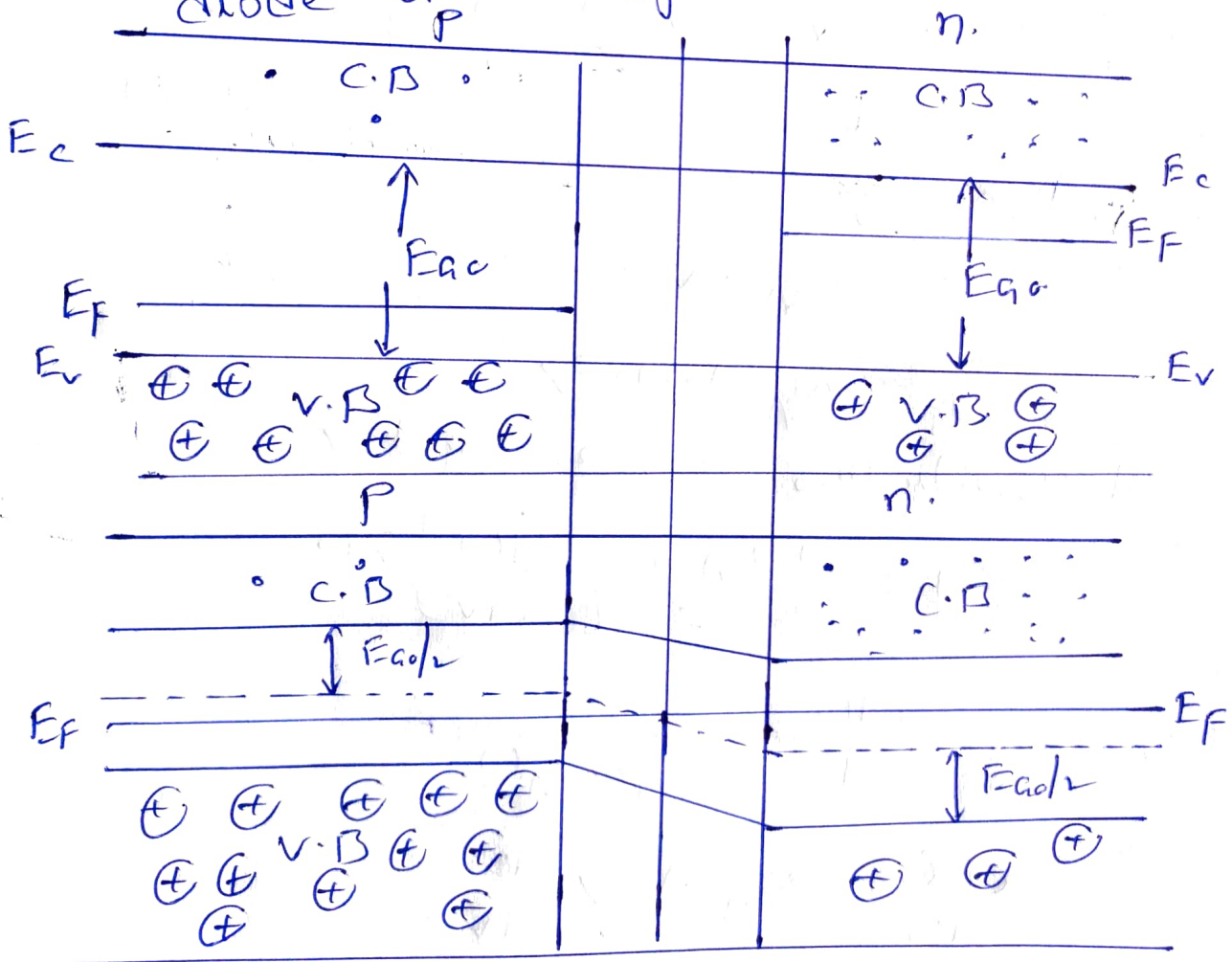
$$\frac{d\phi}{dv} = \frac{\epsilon A}{L} \Rightarrow C_T = \frac{dQ}{dv} = \frac{\epsilon A}{L}$$

$$C_T \propto \frac{1}{L}$$

— 4m

As reverse bias increases the width of the depletion region increases. The Transition Capacitance C_T reduces.

2a) Energy band diagram of PN junction diode under open circuited conditions.



4m

Description about the Energy band diagram before combining and after combining P and n regions. (5)

About Fermi level — 1 m

Junction potential / barrier potential.

$$V_J = V_T \ln \left[\frac{N_A N_D}{n_i^2} \right] \quad \begin{array}{l} N_A = p_p \\ N_D = n_n \end{array}$$

$$V_T = kT$$

$$\therefore \boxed{V_J = V_T \ln \left[\frac{p_p}{p_n} \right]} \quad \boxed{V_J = V_T \ln \left[\frac{n_n}{n_p} \right]}$$

— 3 m

2b) Diffusion capacitance:

During forward bias condition another capacitance comes into existence called as Diffusion capacitance. C_D

→ let us assume the P-n Junction diode in which p-side is heavily doped when compared to n-side.

Hence the majority charge carriers which constitute the total current is holes.

→ We know that the current equation is given as (6)

$$I = I_{p_n}(x) + I_{n_p}(x)$$

Here the current is mainly due to holes.

$$I \approx I_{p_n}(x)$$

diffusion current density due to holes is given by

$$J = \frac{I}{A} = -q D_p \frac{dP_n}{dx}$$

$$I(x) = -q A D_p \frac{dP_n(x)}{dx} \quad \text{--- (1)}$$

$$P_n(x) = P_n(0) e^{-x/L_p} \quad \text{diff wrt. } x.$$

$$\frac{dP_n(x)}{dx} = P_n(0) \frac{d}{dx} \left(e^{-\frac{x}{L_p}} \right)$$

$$= P_n(0) e^{-\frac{x}{L_p}} \left(-\frac{1}{L_p} \right)$$

$$\text{at } x=0 \\ = -\frac{P_n(0)}{L_p}$$

$$\therefore I(x) = -q A D_p \frac{P_n(0)}{-L_p}$$

$$I = q A \frac{D_p}{L_p} P_n(0) \quad \therefore P_n(0) = \frac{I L_p}{q A D_p}$$

The excess charge Q exists on n side is given by

$$Q = \int_0^{\infty} q A P_n(0) e^{-x/L_p} dx$$

$$\therefore \phi = \gamma P_n(0) \left[\begin{matrix} e^{-x/L_p} \\ -\frac{x}{L_p} \end{matrix} \right]_0^{\infty}$$

$$\phi = \gamma A L_p P_n(0)$$

$$\phi = \frac{L_p^2 I}{D_p} \quad \therefore \gamma = \frac{L_p^2}{D_p}$$

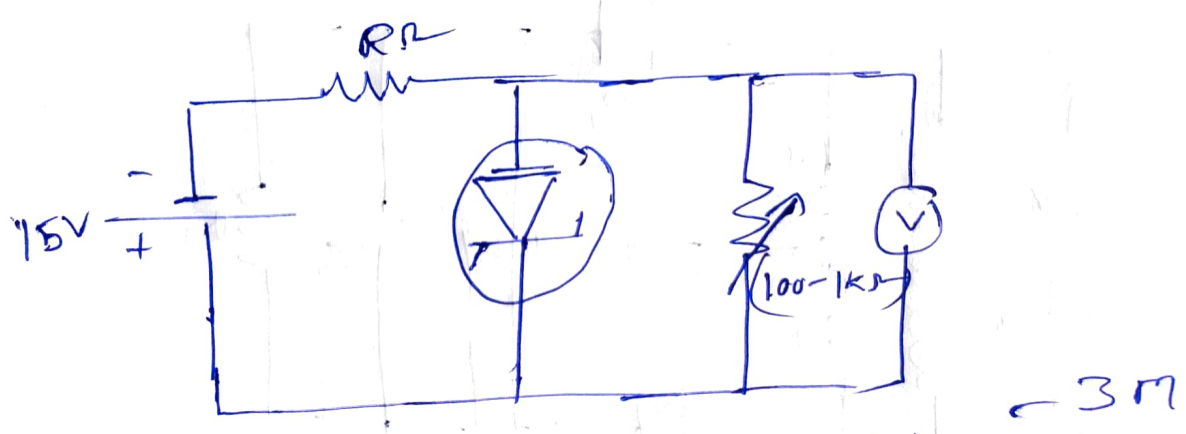
$$\phi = \gamma I \quad C_D = \frac{d\phi}{dV} = \frac{d\phi}{dI} \times \frac{dI}{dV}$$

$$\frac{d\phi}{dI} = \gamma \quad I = I_0 \left[e^{V/nV_T} - 1 \right]$$

$$\frac{dI}{dV} = \frac{I_0 e^{V/nV_T}}{nV_T} = \frac{I}{nV_T}$$

$$\therefore \left[C_D = \frac{d\phi}{dI} \times \frac{dI}{dV} = \frac{\gamma I}{nV_T} \right]$$

3a) Zener diode as voltage regulator.



In the reverse bias condition

Zener diode is used as voltage regulator in reverse bias condition. (8)

→ Apply a fixed reverse bias voltage and vary the potential across the Zener diode. then the voltage across the load remains almost unchanged for variable resistances

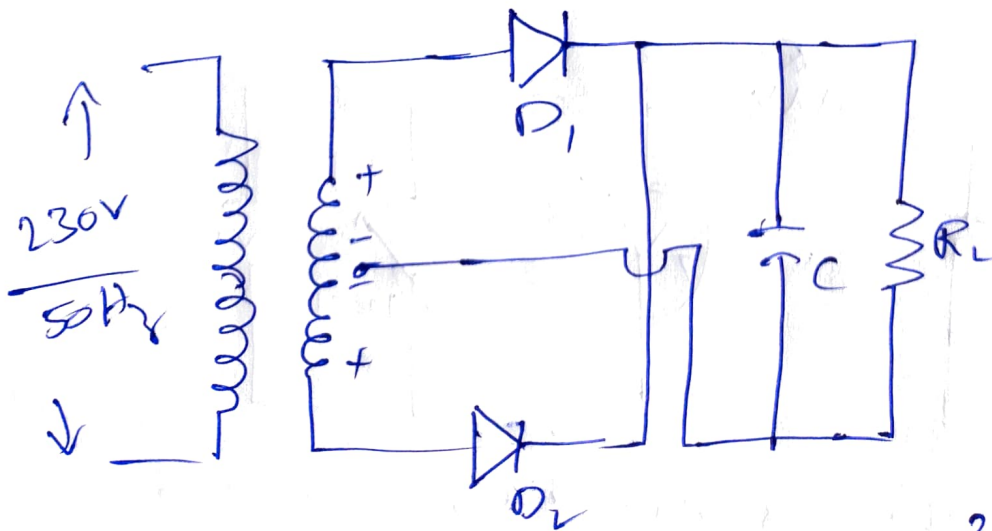
$$\%R = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100. \quad \begin{array}{l} - 3m \\ - 1m \end{array}$$

$V_{NL} \rightarrow V_{\text{No load}}$

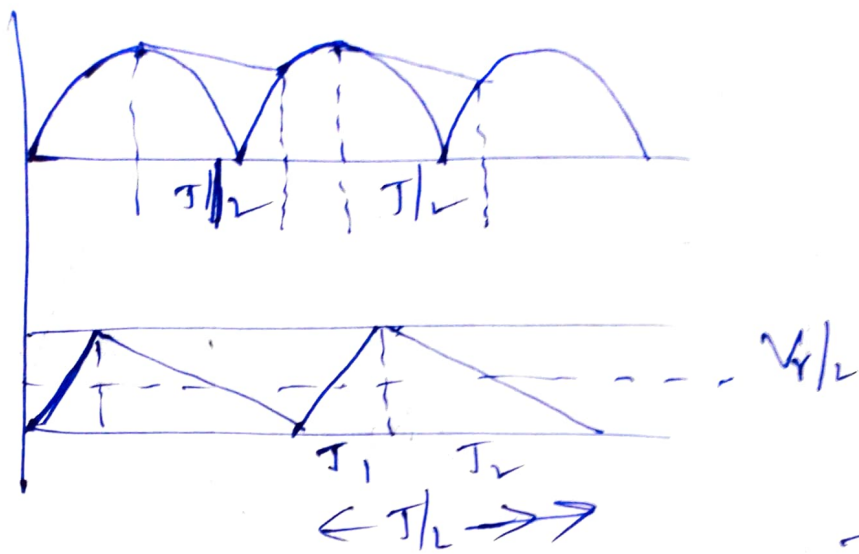
$V_{FL} \rightarrow V_{\text{Full load}}$

3b)

Full wave rectifier with capacitive filter



- 2m



ripple factor $\gamma = \frac{V_{rms}}{V_{dc}}$ for triangular waveform $V_{rms} = \frac{V_r}{2\sqrt{3}}$

$Q = CV_r$ $Q = \int_0^{T/2} i_L dt = I_{dc} T/2$

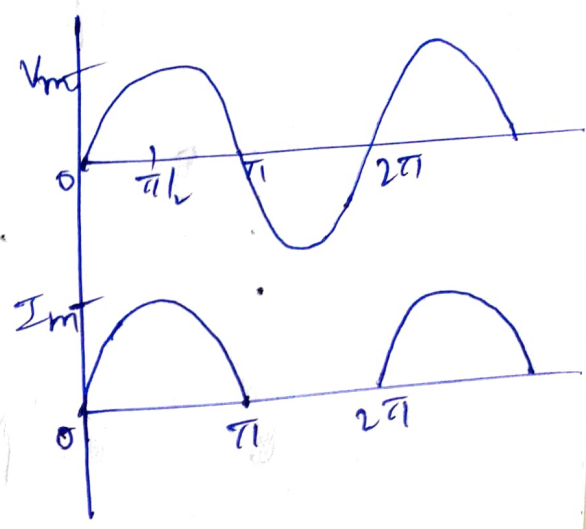
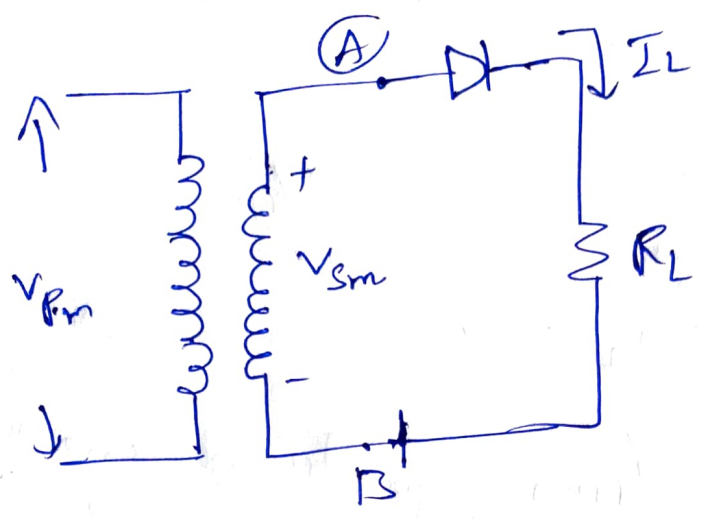
$Q = I_{dc} \cdot \frac{T}{2} \therefore CV_r = I_{dc} \frac{T}{2}$

$\therefore V_r = \frac{I_{dc} T}{2C}$ $I_{dc} = \frac{V_{dc}}{R_L}$

$\therefore V_{rms} = \frac{V_{dc}}{2fR_L C 2\sqrt{3}} \Rightarrow \frac{V_{rms}}{V_{dc}} = \gamma$

$\gamma = \frac{1}{4\sqrt{3} f R_L C}$ 3m

4a) Block diagram of Halfwave rectifier:



$$V_{Sm} = V_m \sin \omega t.$$

$$I_L = I_m \sin \omega t. \quad (0 \leq \omega t \leq \pi)$$

$$= 0 \quad (\pi \leq \omega t \leq 2\pi)$$

$I_m \rightarrow$ Peak value of load current

$$I_{DC} = \frac{1}{2\pi} \int_0^{2\pi} I_L \, d\omega t.$$

$$= \frac{1}{2\pi} \left[\int_0^{\pi} I_m \sin \omega t \, d\omega t + \int_{\pi}^{2\pi} I_m \sin \omega t \, d\omega t \right]$$

$I_L = 0.$

$$I_{DC} = \frac{I_m}{2\pi} [-\cos \omega t]_0^{\pi}$$

$$I_{DC} = \frac{I_m}{2\pi} (2) \Rightarrow \boxed{I_{DC} = \frac{I_m}{\pi}}$$

Rms value of the load current

$$I_{RMS} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} I_L^2 \, d\omega t.}$$

$$I_{RMS} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} I_m^2 \sin^2 \omega t \, d\omega t}$$

$$I_L = I_m \sin \omega t \quad 0 \leq \omega t \leq \pi$$

$$= 0 \quad \pi \leq \omega t \leq 2\pi$$

$$\therefore I_{RMS} = \sqrt{\frac{I_m^2}{2\pi} \int_0^{\pi} \left[\frac{1 - \cos 2\omega t}{2} \right] d\omega t}$$

$$I_{RMS} = \sqrt{\frac{I_m^2}{2\pi} \left(\frac{\omega t}{2} - \frac{\sin 2\omega t}{4} \right)_0^{\pi}} = \frac{I_m}{2}$$

Ripple factor $\gamma = \frac{I_{ac}}{I_{dc}}$

$$I_{ac} = \sqrt{I_{RMS}^2 - I_{dc}^2} \quad \therefore \gamma = \sqrt{\frac{I_{RMS}^2 - I_{dc}^2}{I_{dc}^2}}$$

$$\gamma = \sqrt{\frac{\left(\frac{I_m}{2}\right)^2}{\left(\frac{I_m}{\pi}\right)^2} - 1} = \sqrt{\frac{\pi^2}{4} - 1} = \underline{\underline{1.21}}$$

4b) working principle of varactor Diode

→ As the transition capacitance of a diode varies with the applied voltage, it can be used as voltage variable capacitance in many applications.

→ The diodes which show the transition capacitance property predominantly is called varactor diodes.

$$C_T = \frac{k}{(V_J + V_R)^n}$$

$k = \text{const}$ depends on Semiconductor.

$V_J = \text{Junction potential.}$

$V_R = \text{reverse bias voltage.}$

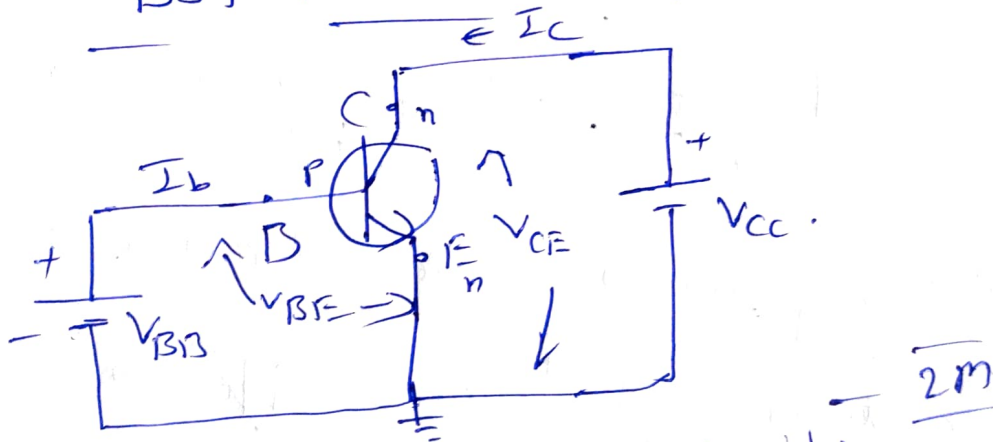
$n = 1/2$ for alloy junction

$= 1/3$ for diffused junction 2M

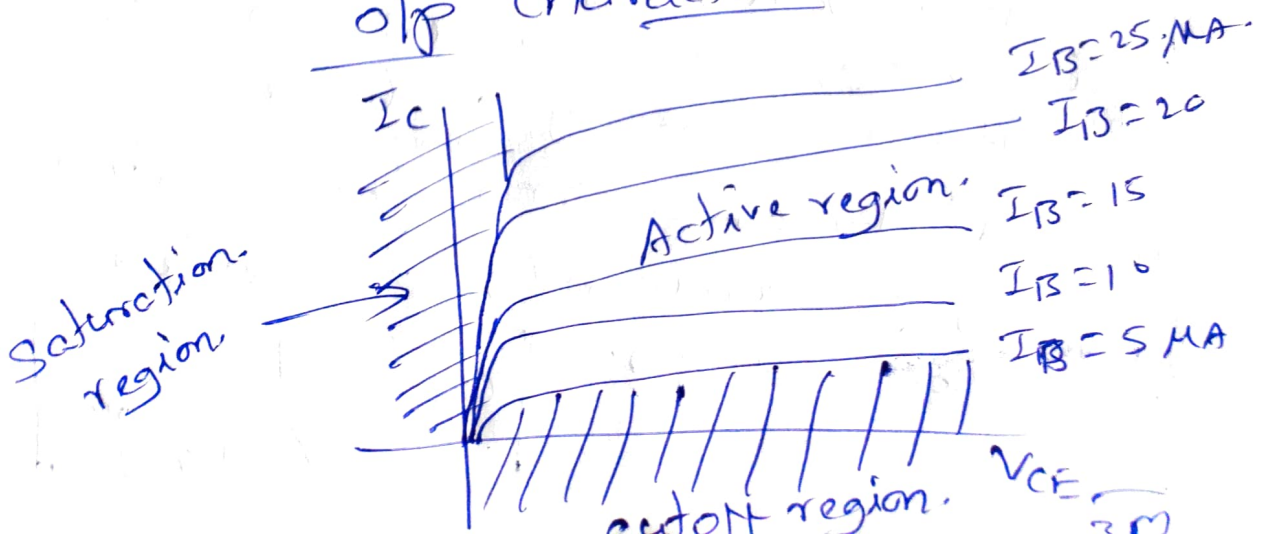
Applications:

- ① Tuned circuits
- ② FM modulator
- ③ Automatic frequency control devices.
- ④ Television receivers 3M

5a) BJT in C-E Configuration



o/p characteristics:

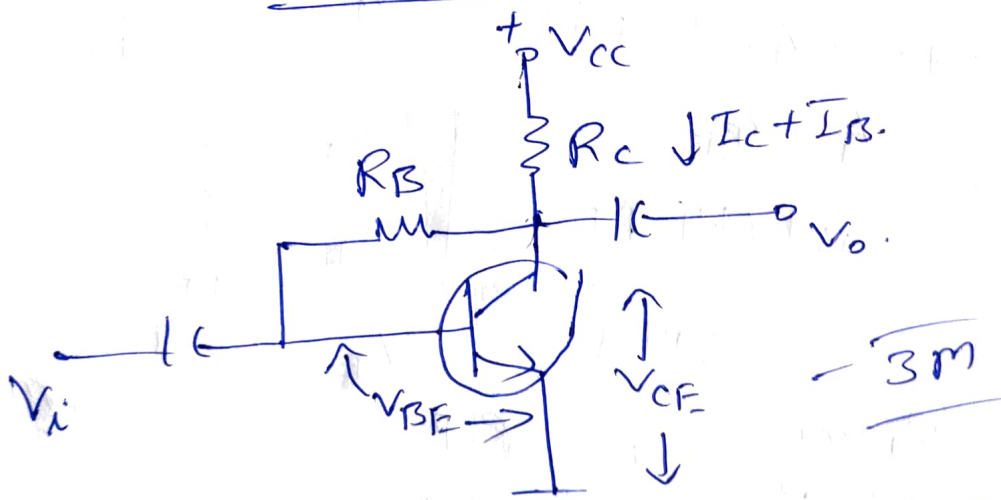


J_E	J_C	Region of operation
F.B	F.B	Saturation
F.B.	R.B	Active.
R.B	R.B	cut off

$F.B \rightarrow$ Forward Bias
 $R.B \rightarrow$ reverse bias.
 $J_E \rightarrow$ Emitter base J_n
 $J_C \rightarrow$ collector base J_n .

2M

5b) collector to base Bias:



3M

Applying KVL to Base circuit

$$V_{CC} - (I_B + I_C)R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} = (R_B + R_C)I_B + I_C R_C + V_{BE}$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta)R_C}$$

$$I_C = \beta I_B$$

2M

Applying KVL to collector circuit

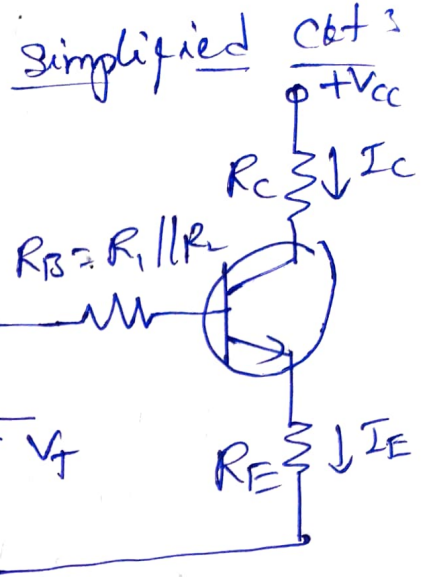
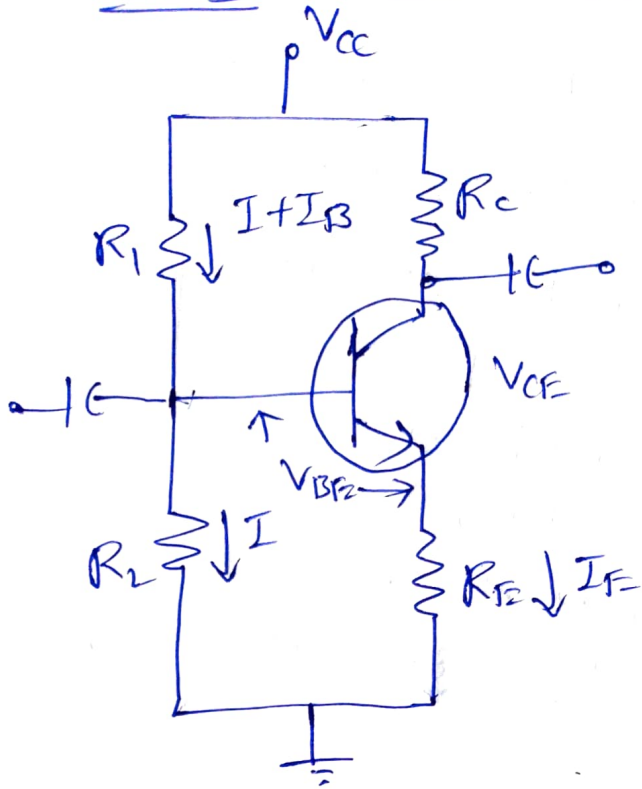
$$V_{CC} - (I_C + I_B)R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - (I_C + I_B)R_C$$

Q point (V_{CE}, I_C)
 (V_{CEQ}, I_{CQ}) 2M

6a) voltage Divider Bias ckt:

(14)



$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2}$$

$$V_E = V_B - V_{BE}$$

$$I_E = \frac{V_E}{R_E}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

Applying KVL to b-g-e ckt:

$$V_T = I_B R_B + V_{BE} + I_E R_E$$

$$\therefore I_B = \frac{V_T - V_{BE}}{R_B + (1+\beta)R_E}$$

- 2M

$$V_T = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

diff w.r to I_C

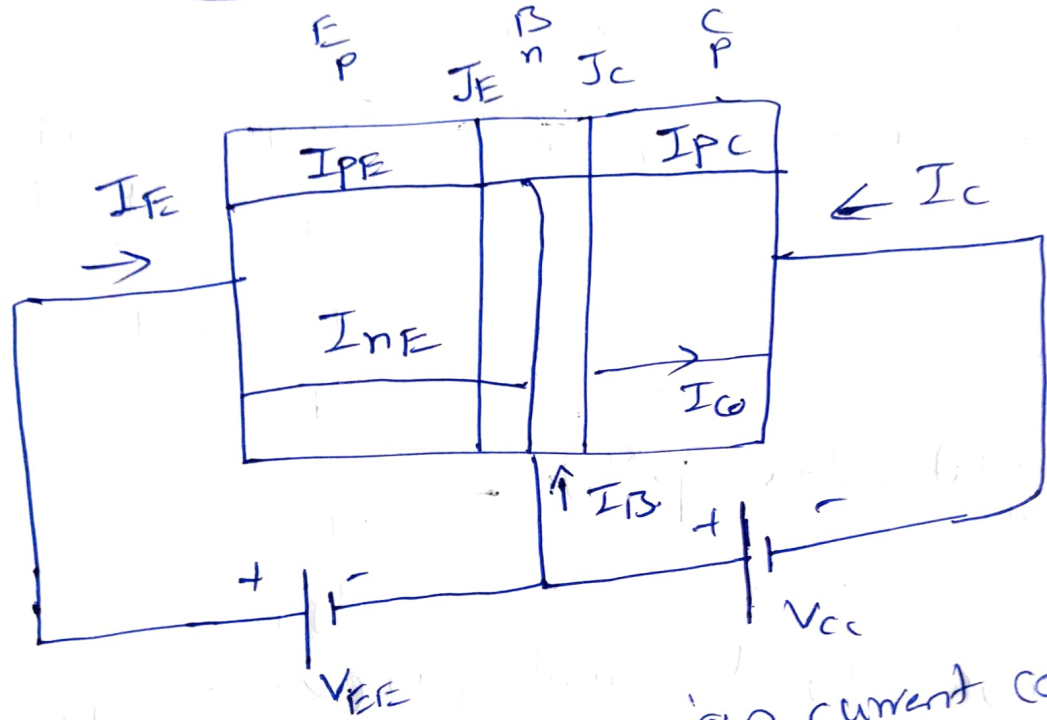
$$0 = \frac{\partial I_B}{\partial I_C} \times R_B + \frac{\partial I_B}{\partial I_C} \times R_E + R_E$$

$$\therefore \frac{\partial I_B}{\partial I_C} = -\frac{R_E}{R_E + R_B}$$

$$S = \frac{1 + \beta}{1 - \beta \left(\frac{\partial I_B}{\partial I_C} \right)} = \frac{1 + \beta}{1 - \beta \left(\frac{R_E}{R_E + R_B} \right)} \approx 1$$

3M

6b) Current components of a PNP Transistor.



→ Figure shows the various current components in the PNP transistor, which flows across the Forward biased Emitter base J_n and Reverse biased collector base $J_n(J_c)$

I_{E_E} consists of I_{P_E} (holes crossing from emitter to base)
 I_{N_E} (electrons crossing from base to emitter)

→ Thus the holes crossing emitter base Junction (J_E) and crossing collector base Junction J_c constitutes the collector current (I_{P_C})

→ If $I_E = 0$ $I_{PE} = 0$ hence I_{PC} becomes 0 (16)
 in such condition. the base and collector acts
 as reverse bias diode and the collector
 current is equal to the reverse saturation
 current I_{CO} .

$$\therefore I_C = -I_{PC} + I_{CO} \quad \underline{4M}$$

Parameters of transistor:

① Emitter efficiency (γ) = $\frac{I_{PE}}{I_E} = \frac{I_{PE}}{I_{PC} + I_{PE}}$
 $\approx \frac{I_{PE}}{I_{PE}} \approx 1$

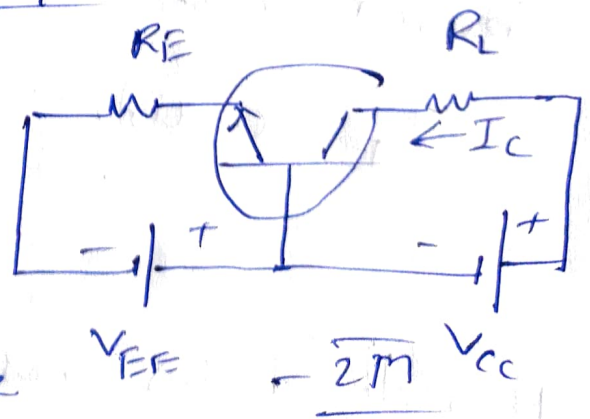
② Transport factor (β^{*}) = $\frac{I_{PC}}{I_{PE}}$

③ Large signal current gain (α) = $\frac{I_{PE}}{I_E}$
 $\underline{3M}$

2a) Transistor as an Amplifier:

→ a small voltage change
 ΔV_i between emitter
 and base causes a
 relatively large
 emitter current change

$$\Delta I_E \quad \underline{2M}$$



→ Therefore the change in the output current is $\propto \Delta I_E$ and the change in the output voltage across the load resistor $\Delta V_o = \underline{\underline{\alpha' R_L \Delta I_E}}$

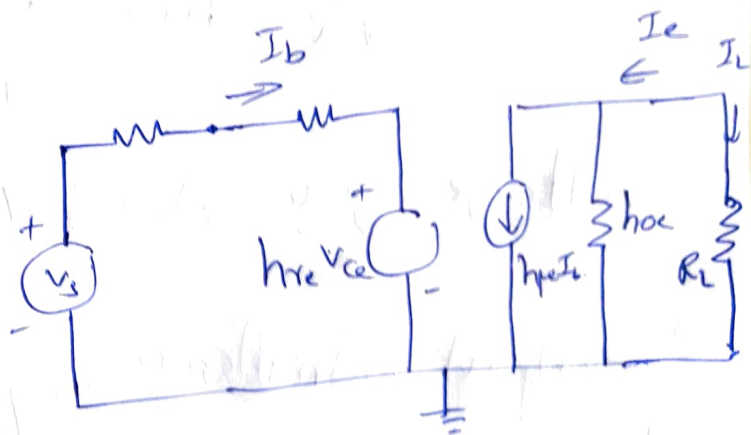
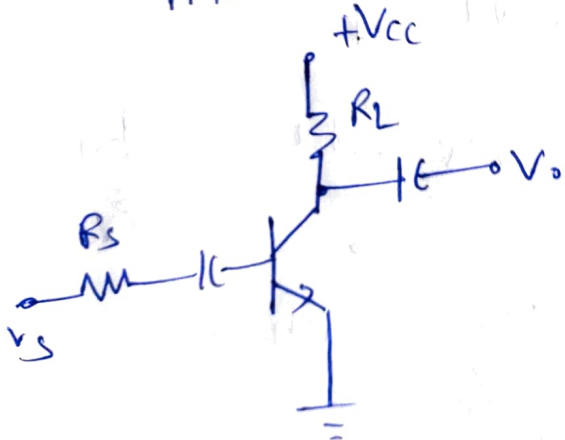
$$\Delta V_i = r_e' \Delta I_E$$

$$A = \frac{\Delta V_o}{\Delta V_i} = \frac{\alpha' R_L \Delta I_E}{r_e' \Delta I_E} = \alpha' \frac{R_L}{r_e'}$$

let us assume $r_e' = 40 \Omega$ $\alpha' = 1$ $R_L = 2k\Omega$

$$\underline{\underline{A = 50}} \quad \underline{\underline{30M}}$$

7b) Derive the expressions for A_i' , A_v , R_i and R_o for CE Amplifier using h-parameter model.



$$\underline{\underline{\text{Current gain } A_i'}} = \frac{I_c}{I_b} = + \frac{I_c}{I_b}$$

$$I_c = h_{fe} I_b + h_{oe} v_c$$

$$I_c = h_{fe} I_b + h_{oe} (-I_c R_L)$$

$$\therefore (1 + h_{oe} R_L) I_c = h_{fe} I_b$$

$$\Rightarrow \frac{I_c}{I_b} = \frac{h_{fe}}{1 + h_{oe} R_L}$$

$$A_i = - \frac{I_c}{I_b} = - \frac{h_{fe}}{1 + h_{oe} R_L}$$

$$\underline{\text{Input resistance}} (R_i) = \frac{V_b}{I_b}$$

$$V_b = h_{ie} I_b + h_{re} V_c$$

$$V_c = -I_c R_L = A_i I_b R_L$$

$$\therefore R_i = \frac{h_{ie} I_b + h_{re} A_i I_b R_L}{I_b}$$

$$R_i = h_{ie} + h_{re} A_i R_L$$

$$R_i = h_{ie} - \frac{h_{re} h_{fe} R_L}{1 + h_{oe} R_L}$$

$$\underline{\text{voltage gain}} (A_v): \frac{V_c}{V_b} = \frac{A_i I_b R_L}{V_b} = \frac{A_i R_L}{R_i}$$

$$\underline{\text{output Admittance}}: (Y_o) = \frac{I_c}{V_c} \text{ with } V_s = 0$$

$$I_c = h_{fe} I_b + h_{oe} V_c$$

dividing by V_c

$$Y_o = \frac{I_c}{V_c} = \frac{h_{fe} I_b}{V_c} + h_{oe}$$

with $V_s = 0$

(19)

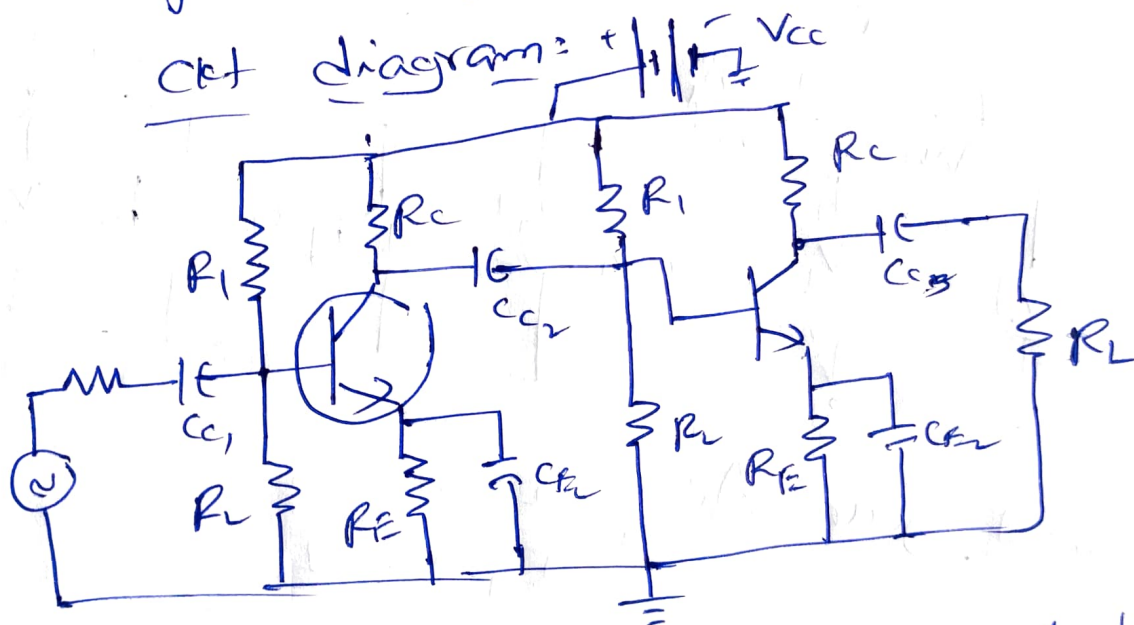
$$R_s I_b + h_{ie} I_b + h_{re} V_c = 0$$

$$(R_s + h_{ie}) I_b = -h_{re} V_c \quad \frac{I_b}{V_c} = \frac{-h_{re}}{R_s + h_{ie}}$$

Substituting value of $\frac{I_b}{V_c}$

$$Y_o = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_s} \quad R_o = \frac{1}{Y_o}$$

8a) Explain the working of a two stage RC coupled amplifier with circuit diagram.

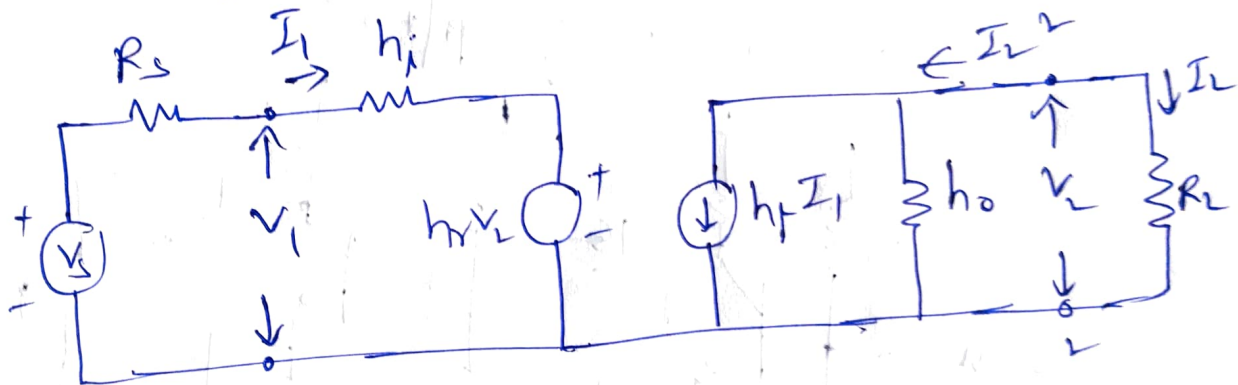
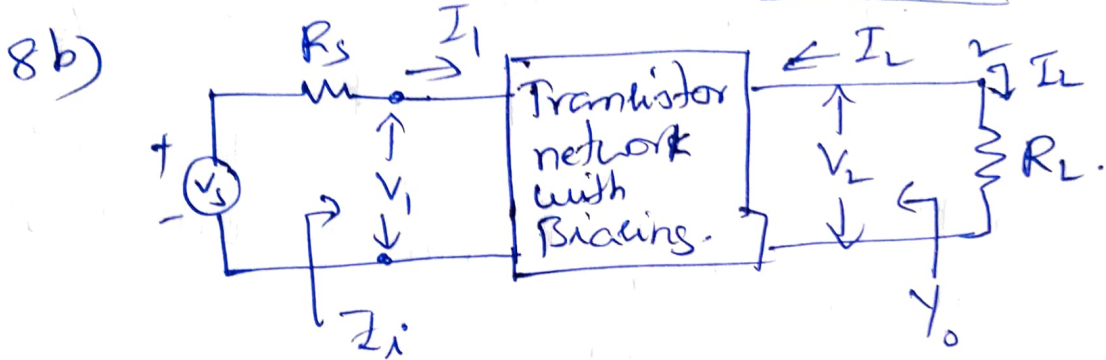


- The o/p of stage 1 is coupled as an input to stage 2.
- The signal is amplified further.
- The first stage CE Amplifier is coupled to second stage CE Amplifier through collector Resistance R_c and.

coupling capacitor C_c , The phase shift (20) of 180° is avoided.

$$A_V = \frac{V_{O2}}{V_S} = \frac{V_{O2}}{V_{i2}} \times \frac{V_{O1}}{V_S}$$

$$= \underline{A_{V2} \times A_{V1}}$$



current gain $A_i = \frac{I_2}{I_1} = -\frac{I_2}{I_1}$

$$I_2 = h_f I_1 + h_o V_2 \quad V_2 = -I_2 R_L$$

$$I_2 = h_f I_1 + h_o (-I_2 R_L)$$

$$I_2 + h_o I_2 R_L = h_f I_1$$

$$(1 + h_o R_L) I_2 = h_f I_1$$

$$\boxed{\frac{I_2}{I_1} = \frac{h_f}{1 + h_o R_L}}$$

Current Gain (A_{i_s})

Input Impedance (Z_i) / (R_i)

$$R_i = \frac{V_1}{I_1} \quad V_1 = h_i I_1 + h_r V_2$$

$$\therefore R_i = h_i + h_r \frac{V_2}{V_1}$$

$$V_2 = -I_2 R_L = A_i I_1 R_L$$

$$R_i = h_i + h_r \frac{A_i I_1 R_L}{I_1} = h_i + h_r A_i R_L$$

$$A_i = \frac{-h_f}{1 + h_o R_L}$$

$$Z_i \text{ or } R_i = h_i - \frac{h_f h_r R_L}{1 + h_o R_L}$$

Voltage Gain (A_v)

$$A_v = \frac{V_2}{V_1} = \frac{A_i I_1 R_L}{V_1} = \frac{A_i R_L}{Z_i}$$

Output Admittance (Y_o)

$$Y_o = \frac{I_2}{V_2} \quad I_2 = h_f I_1 + h_o V_2$$

$$\frac{I_2}{V_2} = \frac{h_f I_1}{V_2} + h_o$$

$$Y_o = h_f \frac{I_1}{V_2} + h_o, \quad R_s + I_1 + h_i I_1 + h_r V_2 = 0$$

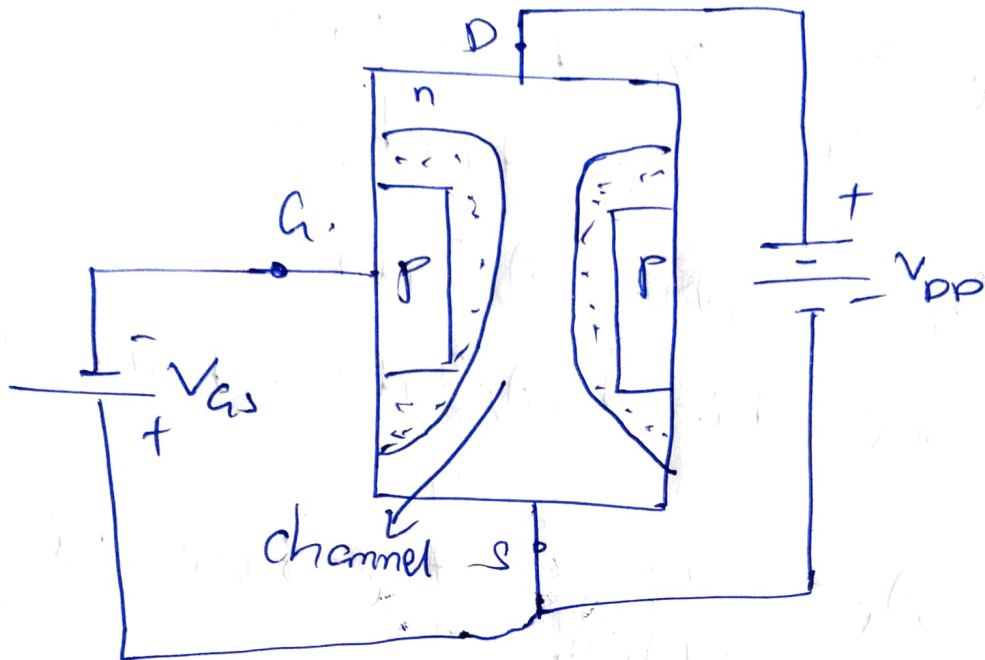
$$\frac{I_1}{V_2} = \frac{-h_f}{R_s + h_i}$$

$$Y_o = h_o - \frac{h_f h_r}{h_i + R_s}$$

9 a)

n-channel JFET

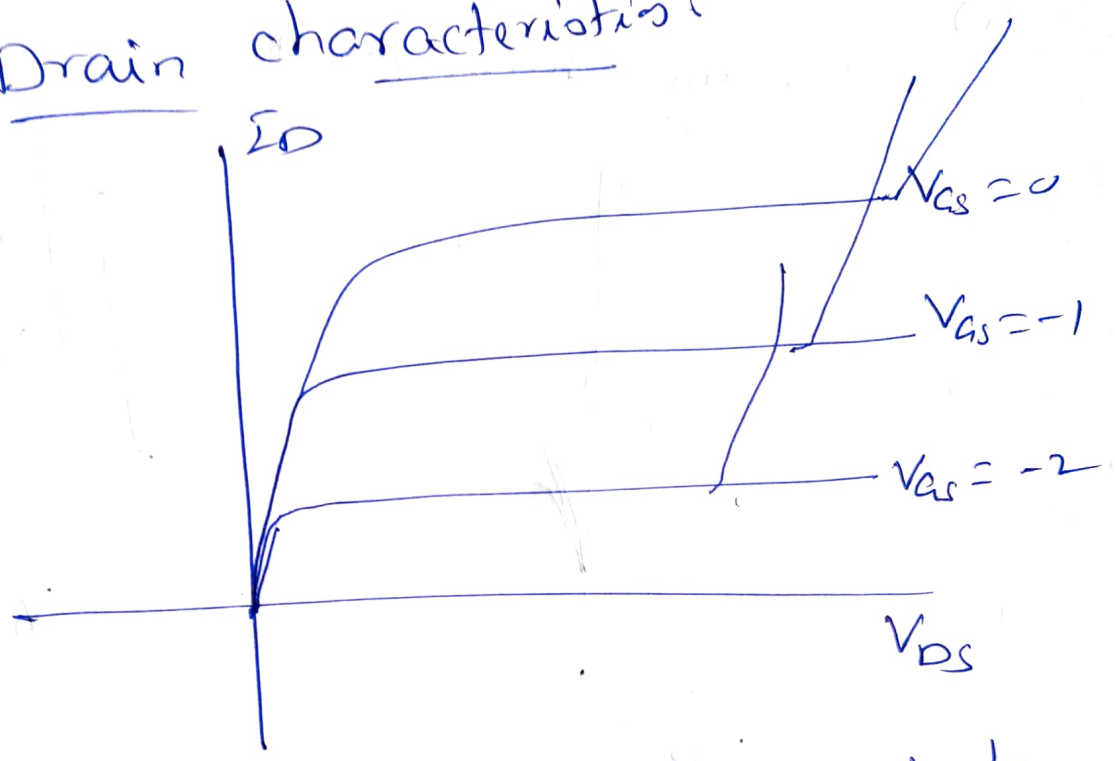
(22)



- The biasing voltage V_{GS} is applied between Source and Drain.
- when V_{GS} is applied the electrons from metallic wire enters into source (S) and the electrons from the source travel towards the Drain (D) as the Drain terminal is positive.
- As the V_{DS} increases the flow of electrons from ~~them~~ source to Drain increases and flow through the channel.
- As the width of the channel is limited the current is limited at

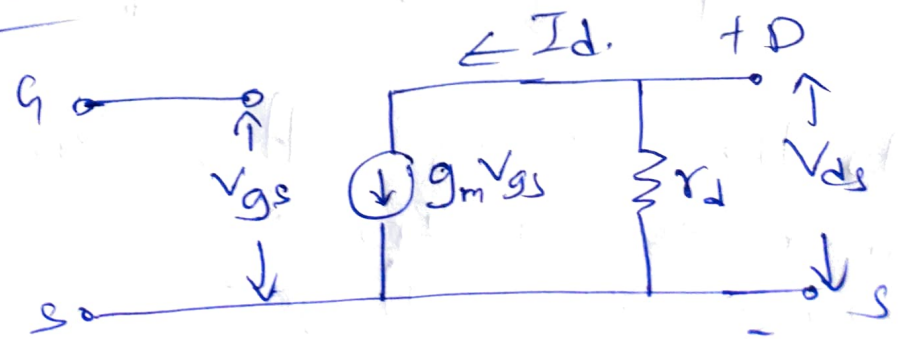
Particular drain to source voltage V_{DS} the voltage at which the drain current I_D becomes constant is called "pinch-off voltage V_p "

Drain characteristics?



→ if the reverse voltage across gate to source V_{GS} increases, the channel width is reduced due to increased in depletion region in the n type substrate.

9b) Fixed bias method n channel JFET

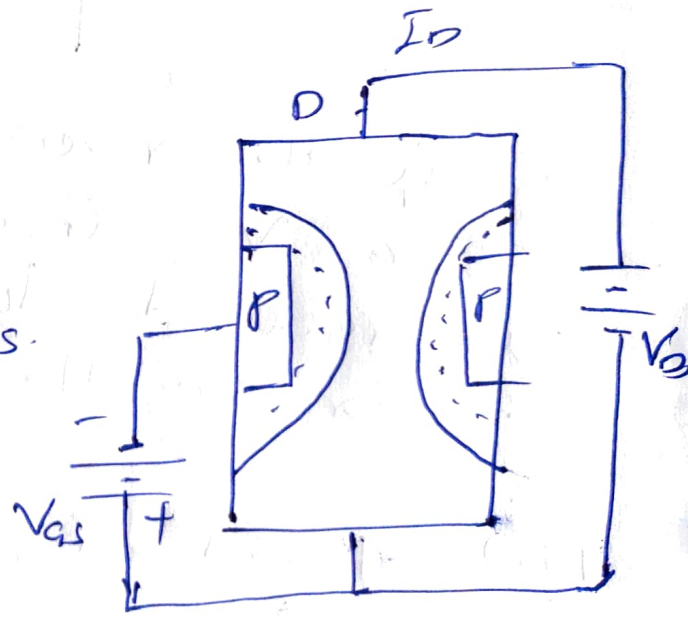
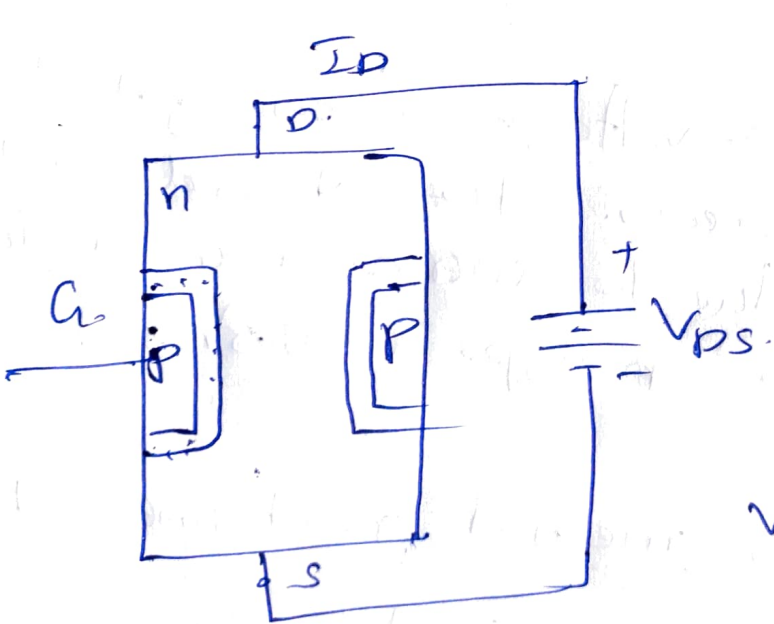
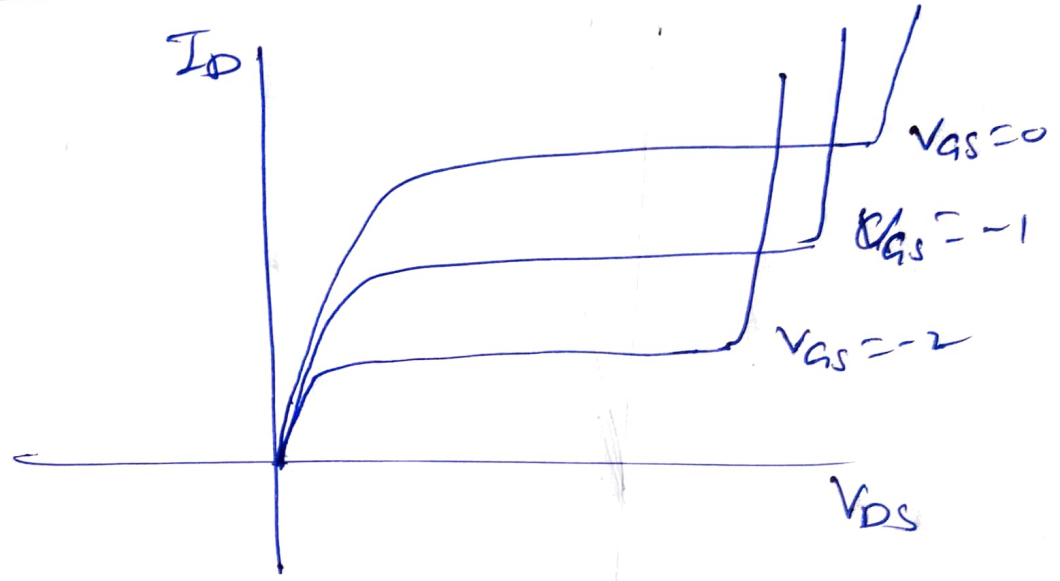


$$\Delta I_D = g_m \Delta V_{GS}$$

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \Big|_{V_{GS} = \text{const}}$$

10 a)

Drain characteristics.

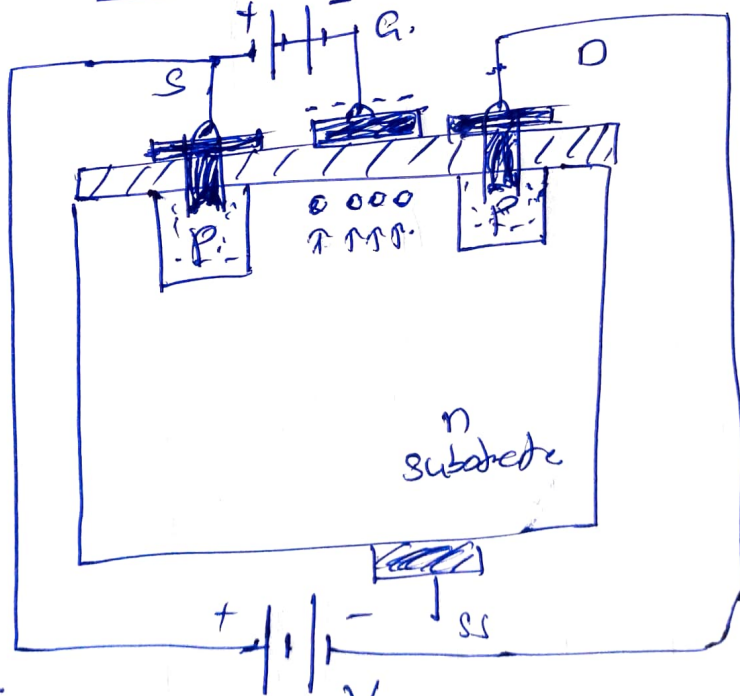


→ As the biasing voltage V_{DS} increases the drain current I_D increases until the pinch off voltage.

if the gate to source voltage V_{GS} increases the negative bias at V_{GS} increases and hence the width of the depletion layer between p and n regions increases thus the channel width is reduced.

→ Hence even though the drain to source voltage V_{DS} increases the drain current remains constant as the width of the channel is limited.

10b) p-channel Enhancement MOSFET:



Prepared by
N.V. Maheshwari
Asst professor
ECE Dept

